A 120-GHz Millimeter-wave MMIC Chipset for Future Broadband Wireless Access Applications

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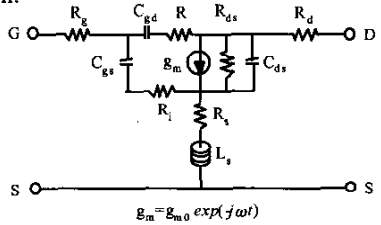
Abstract — **A flexible CPW-MMIC (coplaner-waveguide monolithic microwave integrated circuit) chipset has been fabricated for 120-GHz future broadband wireless systems. The power amplifier has small signal gain of 8.5 dB from 115 to 135 GHz. The 1-dB compression point is 3 dBm at 120 GHz. We employed a traveling wave switch configuration for the ASK modulator. The insertion loss of the switch is less than 1.5 dB and the on-off ratio is more than 13.5 dB at 120 GHz. For the ASK modulator-demodulator chipset, the measured BER is 1e-10 for 10-Gbit/s PRBS 2^{11}-1 data at -13 dBm input power and 120-GHz RF frequency. The frequency doubler has an output power of -11 dBm at 120 GHz with fundamental and harmonics rejection better than 30 dBc.**

I. INTRODUCTION

The frequency region above 100 GHz is being explored to meet the strong demand for high-transmission-rate wireless applications. We have already reported a successful trial of wireless communication above 100 GHz by means of photonic techniques [1]. The upper half of the F waveguide frequency band (115-140 GHz) is well suited for such a purpose, because of the ease of hardware implementation, sufficient bandwidth for large data capacity, and moderate attenuation caused by oxygen absorption.



(a)

$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	$R_{ds}(\Omega)$	$R_i(\Omega)$	$R_j(\Omega)$
4.75	8.54	16.4	616	6.54	62.1
C_{gs}(fF)	C_{gd}(fF)	C_{ds}(fF)	g_{m0}(mS)	τ(ps)	L(pH)
25	3.3	3.9	29	0.14	8.2

(b)

Fig. 1. FET model and parameters. The gate length and the width are 0.1 and 20 μm, respectively. (a) Equivalent circuit. (b) Parameters at V_{gs} = 0 V, V_{ds} = 1.5 V.

Moreover, we can make the system quite compact because the antenna and other passive components can be made small. A compact and broadband transceiver will be a key to the future large-capacity wireless access systems. This frequency range also has the potential for use in very broadband local-area communication links in high-density areas.

In this paper, we present a flexible CPW-MMIC (coplaner-waveguide monolithic microwave integrated circuit) chipset for future 120-GHz broadband wireless systems. A 0.1-μm-gate InAlAs/InGaAs HEMT [2, 3] was used with a MIM capacitor and double-layer interconnection process. The device typically has a unity current gain frequency f_t of 170 GHz and a maximum oscillation frequency f_{max} of 350 GHz. Maximum transconductance is 1.2 S/mm at DC.

II. DEVICE MODELING

A small-signal equivalent circuit is used to study the stability and matching condition of the circuit. The S-parameters from 45 MHz to 110 GHz were obtained using HP8510XF before the fitting procedure. Figures 1(a) and (b) show the equivalent circuit of the FET and the parameters for a 20-μm gate FET, respectively.

The circuits have to be designed for frequencies above the measured frequency range of the S-parameters. To improve the accuracy of device parameters at the operating frequencies, we simultaneously used S-parameters obtained not only from common-source but also common-gate configurations for the parameter extraction. After removing pad parasitics by a de-embedding technique, the S-parameters of the model were fit to the measured one. The cost functions for common-source (C_{SC}) and common-gate (C_{GC}) were combined into a final cost function (C_{final}) by the following formula.

$$C_{SC}=\left[\frac{1}{n}\sum_{i=1}^{2}\sum_{j=1}^{2}\sum_{l=1}^{n}\frac{\left|S'_{Slij}-S^{*}_{Slij}\right|^{2}}{\left|S^{*}_{Slij}\right|^{2}}\right]^{\frac{1}{2}} \quad (1)$$

$$C_{GC}=\left[\frac{1}{n}\sum_{i=1}^{2}\sum_{j=1}^{2}\sum_{l=1}^{n}\frac{\left|S'_{Glij}-S^{*}_{Glij}\right|^{2}}{\left|S^{*}_{Glij}\right|^{2}}\right]^{\frac{1}{2}} \quad (2)$$

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$$C_{final} = \sqrt{C_{SC}^2 + C_{GC}^2} \qquad (3)$$

where

n = Number of frequency data points,

S'_S = Modeled S-parameters for common-source FET,

S'_G =Modeled S-parameters for common-gate FET,

S''_S = Measured S-parameters for common- source FET,

S''_G =Measured S-parameters for common-gate FET.

The fitting parameter values were modified to minimize the C_{final}. Figures 2(a), (b) and (c) shows the calculated C_{final} versus fitting parameters C_{gs}, C_{gd}, and C_{ds} around the optimized values. The cost function and capacitance were normalized by the optimized values. For comparison, the fitting results minimizing C_{SC} or C_{GC} are also indicated. It is clear in Fig. 2(c) that the sensitivity for C_{ds} is dramatically improved by using the cost function C_{final} compared with C_{SC} which has been conventionally used for parameter extraction.

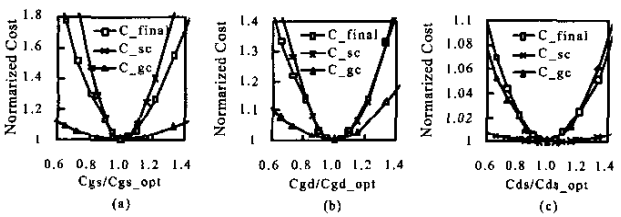

Fig. 2. Normalized cost vs parameter C_{gs}, C_{gd} and C_{ds} using different cost functions.

A small-signal equivalent circuit for noise model was also made at V_{gs} = 0 V and V_{ds} = 0.95 V by the method discussed above. The Pospieszalski noise model has been used [4], i.e. two frequency-independent equivalent noise temperatures T_g and T_d were determined for Ri and R_{ds}, respectively. It was shown in [4] and [5] that T_g is approximated to be the physical temperature of the device, in this case T_a=300 K. The noise temperature T_d was used to fit the model to noise measurement at 15 GHz.

Large-signal simulation was performed by using a MESFET model in HSPICE for various bias conditions. The HSPICE parameters were extracted using the conventional method, namely, I-V curve fitting and S-parameter fitting up to 110 GHz.

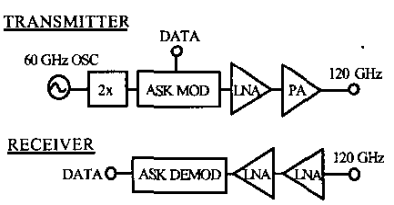

Fig. 3. The block diagram of the front-end.

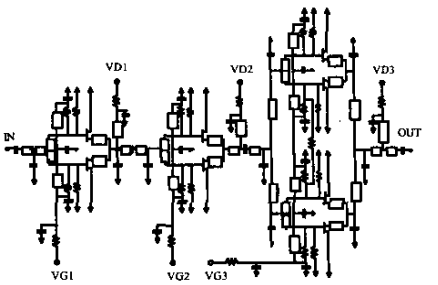

Fig. 4. The equivalent circuit of the power amplifier.

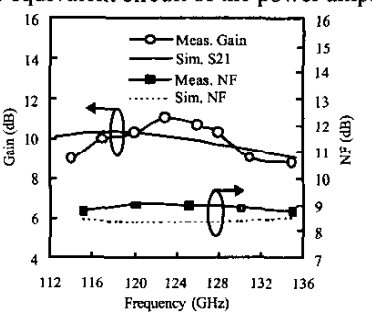

Fig. 5 Measured gain and NF of the amplifier (Gain: $VG_{1\text{-}3}$=0 V, $VD_{1\text{-}3}$=1.7 V, NF: $VG_{1\text{-}3}$=0 V, VD_1=1.2 V, $VD_{2\text{-}3}$=1.7 V.)

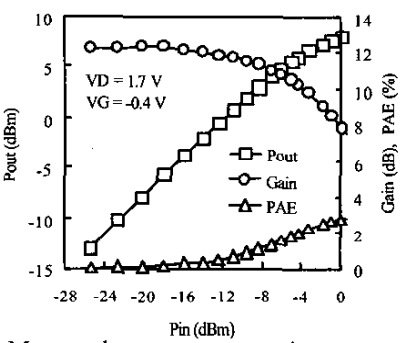

Fig. 6. Measured output versus input power of the amplifier ($VG_{1\text{-}3}$=0 V, $VD_{1\text{-}3}$=1.7 V).

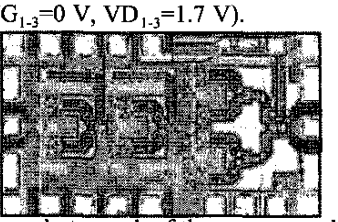

Fig. 7. A microphotograph of the power amplifier.

III. MMIC CHIP SET & RESULTS

Transceiver Configuration

A block diagram of 120-GHz broadband wireless access front-end is shown in Fig. 3. We made the transceiver configuration as simple as possible [6] to maintain high data rate and ease of hardware

implementation.

Power Amplifier

Figure. 4 shows the equivalent circuit of the power amplifier. This amplifier has a three-stage configuration with 4 x 20 μm, 4 x 20 μm, and 8 x 20-μm HEMTs. To retain device performance, 20-μm-gate-width FETs were used in a tournament configuration. We employed a band-pass filter-type matching circuit with a stabilizing-resister in the gate. An isolation-resistor is located between each 2 x 20 μm FET cell in the final stage. RC filters in the drain bias circuit prevent unintentional oscillation at low frequency. Figures 5 and 6 show the measured performance of the amplifier. The output power is more than 8 dBm and the 1-dB compression point is 3 dBm at 120 GHz at $VD_{1\text{-}3}$ =1.7 V. The small-signal gain is more than 8.5 dB from 115 to 135 GHz at $VD_{1\text{-}3}$ =1.7 V.

Considering use as an amplifier for the receiver for short-range application, the noise figure was measured. The measurement and simulation results are shown in Fig. 5. When it is biased for low NF, 8.9 dB NF with 10-dB associated gain was obtained at 120 GHz. A microphotograph of the fabricated power amplifier is shown in Fig. 7. The intrinsic area of this amplifier is 0.72 mm x 0.44 mm.

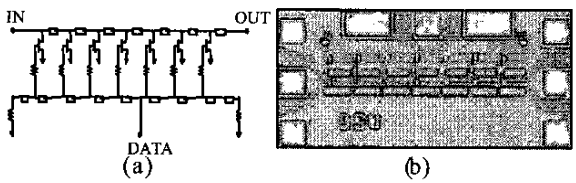

Fig. 8. The equivalent circuit (a) and microphotograph (b) of the ASK modulator.

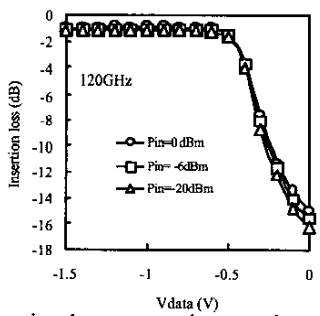

Fig. 9. Insertion loss versus input voltage at the data port of the ASK modulator at 120 GHz.

ASK Modulator

For high-speed modulation and low insertion loss at even over 100 GHz, a traveling wave switch configuration was employed [7]. Figures 8(a) and (b) show the equivalent circuit of the modulator and a microphotograph of the chip. The threshold voltage of the HEMT is -0.5 V, and we assumed a SCFL interface for data input so that a level shift circuit is not required to drive the modulator.

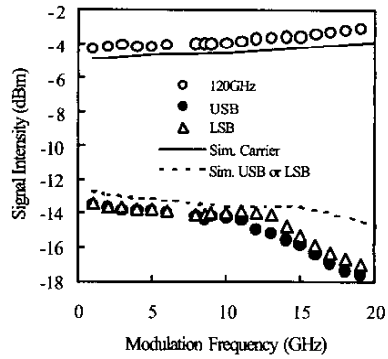

Fig. 10. The side band levels of the ASK modulator. CW signal was applied to the data port. (RF input: 120 GHz, 0 dBm, Data high level =0 V, Data low level=-1.0 V)

Figure 9 shows the data voltage dependency of the insertion loss. Minimum insertion loss is less than 1.5 dB and the on-off ratio is more than 13.5 dB at 0-dBm RF input power. To clarify the switching property, we measured the side band level with CW data input. Figure 10 indicates that the side band level is kept constant below 10-GHz modulation frequency. These results are almost in accordance with the simulation. The switching response is enough to transmit data below 10 Gbit/s. The intrinsic area of the modulator is 0.40 mm x 0.18 mm.

ASK Demodulator

A Schottky barrier diode detector was used as an ASK demodulator. The Schottky barrier gate of HEMTs with 2 x 10 μm gate width was used as a diode. A bias circuit for the diode was also integrated. Below 10 GHz, the measured output return loss is 8 dB. Figure 11 indicates the output voltage of the device at 120-GHz input frequency. The measurements agree with the simulation for both the open circuit and 50-Ω load operations. The sensitivity of the demodulator corresponds to 400 mV/mW for open circuit operation.

In order to test the frequency response of the demodulator, the ASK modulator was directly connected to the demodulator and the bit error rate (BER) was measured (Fig. 12). The measured BER is 1e-10 at -13 dBm input power with the test pattern of a 10-Gbit/s

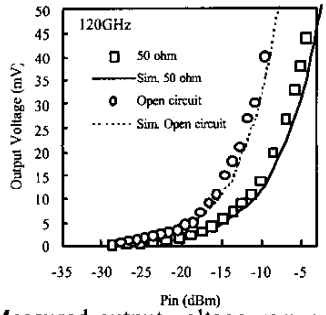

Fig. 11. Measured output voltage versus input power of the ASK demodulator at 120-GHz input.

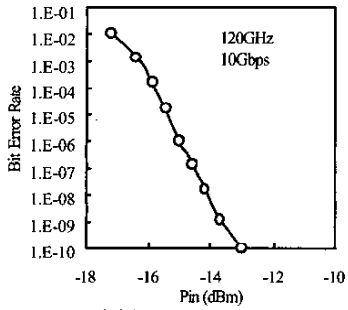

Fig. 12. Measured bit error rate versus input power of the ASK demodulator at 120-GHz input.

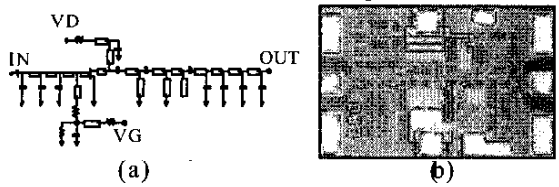

Fig. 13. The equivalent circuit (a) and microphotograph (b) of the doubler.

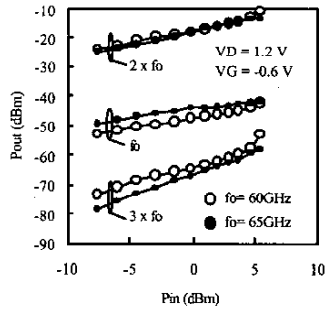

Fig. 14. The output power measurement of the doubler at 60- and 65-GHz fundamental frequency.

pseudo random bit sequence (PRBS) 2^{11}-1. The intrinsic area of the demodulator is 0.46 mm x 0.24 mm.

Frequency Doubler

The doubler MMIC is composed of input and output matching circuits for a 2 x 20 μm HEMT and a band-pass filter at an output port. The equivalent circuit and photograph of the doubler are shown in Fig. 13(a) and (b). The output power was -11 dBm without the output buffer amplifiers at 5 dBm input power as shown in Fig. 14. Figure 14 indicates that fundamental and harmonics rejection is better than 30 dBc at 120- and 130-GHz output frequencies. The intrinsic area of the doubler is 0.42 mm x 0.36 mm.

IV. CONCLUSION

We have described the design and performance of a MMIC chipset for future 120-GHz broadband wireless systems. We developed a power amplifier, an ASK modulator, an ASK demodulator, and a frequency doubler for the data transmission at up to 10 Gbit/s.

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